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Methods Of Forming Materials Between Conductive Electrical Components, And Insulating Materials

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TECHNICAL FIELD

The invention pertains to methods of forming material adjacent electrical components and to methods of forming material between conductive electrical components. The invention further pertains to insulating materials formed adjacent or between conductive electrical components.

BACKGROUND OF THE INVENTION

A prior art semiconductor wafer fragment 10 is illustrated in Fig. 1. Wafer fragment 10 comprises a substrate 12 and conductive electrical components 14, 16 and 18 overlying substrate 12. Conductive electrical components 14, 16 and 18 may comprise, for example, conductive lines. Such conductive lines may be formed from metal, or conductively-doped polysilicon. Between conductive components 14, 16 and 18 is formed an insulative material 20. Material 20 electrically isolates conductive elements 14, 16 and 18 from one another. Insulative material 20 may comprise materials known to persons of ordinary skill in the art, including, for example, silicon dioxide, silicon nitride, and undoped silicon. Although each of these materials has good insulative properties, the materials disadvantageously have high dielectric constants which can lead to capacitive coupling between proximate conductive elements, such as elements 14, 16 and 18. For instance, silicon nitride has a dielectric constant of about 8 and undoped silicon has a dielectric constant of about 11.8.

A prior art method for insulating conductive elements 14, 16 and 18 from one another, while reducing a dielectric constant of a material b tween conductive elements 14, 16 and 18 is illustrated in Figs. 2 and 3. In referring to Figs. 2 and 3, similar numbers to those utilized in Fig. 1 will be used, with differences indicated by the suffix "a" or by different numerals.

Referring to Fig. 2, a semiconductor wafer fragment 10a is illustrated. Fragment 10a comprises a substrate 12a, and overlying conductive lines 14a, 16a and 18a. Between lines 14a, 16a and 18a is a carbon layer 22. Conductive lines 14a, 16a and 18a are inlaid within carbon layer 22 by a damascene method. A thin. gas-permeable, silicon dioxide layer 24 is formed over conductive lines 14a, 16a and 18a, and over carbon layer 22.

Referring to Fig. 3, carbon layer 22 is vaporized to form voids 26 between conductive elements 14a, 16a and 18a. Voids 26 contain a gas. Gasses advantageously have dielectric constants of about 1.

It would be desirable to develop alternative methods for insulating conductive elements from one another with low-dielectric-constant materials.

SUMMARY OF THE INVENTION

The invention encompasses methods of forming insulating materials between conductive elements. The invention pertains particularly to methods utilizing low-dielectric-constant materials for insulating conductive

elements, and to structures encompassing low-dielectric-constant materials adjacent or between conductive elements.

In on aspect, the invention encompasses a method of forming a material adjacent a conductive electrical component. The method includes providing a mass adjacent the conductive electrical component and partially vaporizing the mass to form a matrix adjacent the conductive electrical component. The matrix can have at least one void within it.

In another aspect, the invention encompasses a method of forming a material adjacent a conductive electrical component which includes providing a mass comprising polyimide or photoresist adjacent the conductive electrical component. The method further includes at least partially vaporizing the mass.

In another aspect, the invention encompasses a method of forming a material between a pair of conductive electrical components. The method includes forming at least one support member between the pair of conductive electrical components. The method further includes providing a mass between the at least one support member and each of the pair of conductive electrical components. Additionally, the method includes vaporizing the mass to a degree effective to form at least one void between the support member and each of the pair of conductive electrical components.

In yet another aspect, the invention encompasses an insulating material adjacent a conductive electrical component. The insulating material comprises a matrix and at least one void within the matrix.

In yet another aspect, the invention encompasses an insulating region between a pair of conductive electrical components. The insulating region comprises a support member between the conductive electrical components, the support member not comprising a conductive interconnect. The insulating region further comprises at least one void between the support member and each of the pair of conductive electrical components.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic cross-sectional view of a prior art semiconductor wafer fragment.

Fig. 2 is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary step of a prior art processing method.

Fig. 3 is a view of the Fig. 2 wafer fragment at a prior art processing step subsequent to that of Fig. 2.

Fig. 4 is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary step of a processing method of the present invention.

Fig. 5 is a view of the Fig. 4 wafer fragment shown at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 4 wafer fragment shown at a step subsequent to that of Fig. 5.

Fig. 7 is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary processing step according to second embodiment of the present invention.

Fig. 8 is a view of the Fig. 7 wafer fragment shown at a step subsequent to that of Fig. 7.

Fig. 9 is a diagrammatic cross-sectional view of a semiconductor wafer fragment processed according to a third embodiment of the present invention.

Fig. 10 is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary step of a processing sequence according to a fourth embodiment of the present invention.

Fig. 11 is a view of the Fig. 10 wafer fragment shown at a processing step subsequent to that of Fig. 10.

Fig. 12 is a view of the Fig. 10 wafer fragment shown at a processing step subsequent to that of Fig. 11.

Fig. 13 is a diagrammatic cross-sectional view of a semiconductor wafer fragment processed according to a fifth embodiment of the present invention.

Fig. 14 is a diagrammatic cross-sectional view of a semiconductor wafer fragment processed according to a sixth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A first embodiment of the present invention is described with reference to Figs. 4-6. In describing the first embodiment, like numerals from the preceding discussion of the prior art are utilized where appropriate, with differences being indicated by the suffix "b" or by different numerals.

Referring to Fig. 4, a semiconductor wafer fragment 10b is illustrated. Semiconductor wafer fragment 10b comprises a substrate 12b, and conductive elements 14b, 16b and 18b overlying substrate 12b. Conductive elements 14b, 16b and 18b may comprise, for example, conductive lines. Substrate 12b may comprise, for example, an insulative layer over a semiconductive substrate.

Electrical components 14b, 16b and 18b are horizontally displaced from one another, with electrical components 14b and 18b being laterally outwardly displaced from component 16b. A mass 30 is between electrical components 14b and 16b, and between electrical

components 16b and 18b. Mass 30 is also outwardly adjacent uter conductive lements 14b and 18b.

Mass 30 is preferably an insulative material and may comprise, for example, carbon. Alternatively, by way of example only, mass 30 can comprise polyimide or photoresist. In yet other alternative aspects of the invention, mass 30 can comprise a mixture of a material which is substantially non-vaporizable under selected conditions, and a material which is substantially vaporizable under the selected conditions. Accordingly, complete vaporization of the substantially vaporizable material under the selected conditions will only partially vaporize mass 30. As an example, mass 30 can comprise a mixture of carbon and silicon dioxide. As another example, mass 30 can comprise a mixture of carbon and SiC_x. Preferably, if mass 30 comprises SiC_x, "x" will be from about 0.2 to about 1.5. More preferably, if mass 30 comprises a mixture of carbon and SiC_x, mass 30 will comprise a mixture from about 20% to about 80% carbon, by volume, and from about 80% to 20% SiC_x, by volume, wherein "x" is from about 0.2 to about 1.5.

As will be recognized by persons of ordinary skill in the art, the construction of Fig. 4 may be formed by a number of different methods. For instance, conductive elements 14b, 16b and 18b could be formed first, and mass 30 subsequently deposited over and between conductive elements 14b, 16b and 18b. Mass 30 could then be

planarized to a level approximately equal with upper surfaces of conductive elements 14b, 16b and 18b.

As another example, mass 30 could be deposited between an adjacent conductive lines 14b, 16b and 18b, without being deposited over conductive lines 14b, 16b and 18b.

In yet another example, mass 30 could first be formed over substrate 12b, and subsequently conductive elements 14b, 16b and 18b could be formed within mass 30 by a damascene method. Conductive electrical components 14b, 16b and 18b would thereby effectively be formed within an expanse of mass 30.

If mass 30 comprises carbon, the carbon may be deposited by plasma decomposition of C(n)H(2n) or C(n)H(2n)X(n), wherein "X" is a halogen such as Br, Cl, I, etc. The deposited carbon is preferably about 10,000 Angstroms thick and can be porous. Porosity of a deposited carbon layer can be adjusted by adjusting deposition parameters, such as, plasma power, temperature, pressure, etc.

Referring to Fig. 5, a layer 32 is formed over mass 30, and over conductive elements 14b, 16b and 18b. Layer 32 preferably comprises a gas permeable insulative material and may comprise, for example, silicon dioxide. Layer 32 will preferably be relatively thin, such as about 500 Angstroms thick. If layer 32 comprises silicon dioxide, the layer may be formed, for example, by sputter deposition. As will be discussed below, mass 30 can be partially or substantially totally vaporized after provision of layer 32. Preferably, layer 32 and mass 30

comprise materials which permit mass 30 to be partially or substantially totally vaporized under conditions which do not vaporize layer 32.

Referring to Fig. 6, mass 30 (shown in Fig. 5) is partially vaporized to form a matrix 34 between conductive elements 14b, 16b and 18b. Matrix 34 is also formed outwardly adjacent outer conductive elements 14b and 18b. Matrix 34 can alternatively be referred to as a web, skeleton or scaffolding.

The partial vaporization of mass 30 (shown in Fig. 5) can be accomplished by exposing wafer fragment 10b to an oxidizing ambient at a temperature of from about 200℃ to about 400℃. Appropriate oxidizing ambients include, for example, O_3, plasma O_3, H_2O_2, plasma H_2O_2, combinations of O_3 and H_2O_2, and combinations of plasmia O_3 and H_2O_2. It is thought that the partial vaporization of mass 30 occurs as excited oxygen atoms diffuse through material 32 and volatize material 34. For instance, if material 34 comprises carbon, the material will be converted into a gas comprising CO_2 and/or CO, which can diffuse out through layer 32.

Matrix 34 comprises voids 36. If pores were originally present in layer 30, such pores can expand as mass 30 is vaporized to form voids 36. Preferably, matrix 34 comprises at least one void 36 between each pair of conductive elements. Typically, matrix 34 will comprise a plurality of voids 36 between each pair of conductive elements. The voids and partially vaporized material of matrix 34 provide an insulative material between conductive lines 14b and 16b, and between conductive

lines 16b and 18b, which preferably has a decreased dielectric constant relative to mass 30 (shown in Fig. 5). Accordingly, the conversion of mass 30 to partially vaporized matrix 34 can advantageously decrease capacitive coupling between paired conductive elements 14b and 16b, and between paired conductive elements 16b and 18b. Preferably, matrix 34 has a dielectric constant of less than or equal to about 2.

An advantage of the embodiment discussed above with reference to Figs. 4-6, relative to the prior art method discussed in the "Background" section, is that matrix 34 provides a skeletal support structure in the embodiment of the present invention. Such skeletal support structure can assist in supporting layer 32 over an expanse between paired conductive elements 14b and 16b, and over an expanse between paired conductive elements 16b and 18b. Also, matrix 34 can assist in supporting layer 32 outwardly adjacent outer conductive elements 14b and 18b. Further, due to the supporting properties of matrix 34, layer 32 may be formed either before or after partial vaporization of mass 30 (shown in Fig. 5).

A second embodiment of the present invention is described with reference to Figs. 7-8. In describing the second embodiment, like numerals from the preceding discussion of the first embodiment are utilized, with differences being indicated by the suffix "c" or with different numerals.

Referring to Fig. 7, a semiconductor wafer fragment 10c is illustrated. Wafer fragment 10c comprises a substrate 12c. Conductive

electrical components 14c, 16c and 18c overlie substrate 12c. Electrical components 14c, 16c and 18c are horizontally displaced from one another, with electrical components 14c and 18c being outwardly displaced from component 16c. A mass 30c is between electrical components 14c and 16c, and between electrical components 16c and 18c. Mass 30c is also outwardly adjacent outer conductive elements 14c and 18c. Mass 30c does not comprise carbon, and preferably comprises either polyimide or photoresist. Substrate 12c may comprise, for example, an insulative material over a semiconductive wafer. Conductive elements 14c, 16c and 18c may comprise, for example, metal lines.

A layer 32c is formed over mass 30c, and over conductive elements 14c, 16c and 18c. Layer 32c preferably comprises an insulative material, and may comprise, for example, silicon dioxide. The structure of Fig. 7 is quite similar to the structure of Fig. 5, and may therefore be formed by methods such as those discussed above regarding Fig. 5, with the exception that mass 30c will not comprise carbon.

Referring to Fig. 8, mass 30c (shown in Fig. 7) is substantially totally vaporized to form voids 36c between conductive elements 14c, 16c and 18c, and outwardly adjacent outer conductive elements 14c and 18c. Mass 30c can be substantially totally vaporized by exposing wafer 10c to an oxidizing ambient at a temperature of from about 200°C to about 400°C. The difference between whether a mass, such as mass 30 of Fig. 5, or mass 30c of Fig. 7, is partially vaporized

(as shown in Fig. 6) or substantially totally vaporized (as shown in Fig. 8) can be determined by the time of exposure of a wafer fragment, such as 10b or 10c, to an oxidizing ambient at a temperature of from about 200°C to about 400°C. Such times are readily determinable by persons of ordinary skill in the art.

The second embodiment of the present invention (discussed above with reference to Figs. 7 and 8) differs from the prior art method of discussed above in the Background section in that the second embodiment utilizes an insulative layer 30c which does not comprise carbon, such as a layer of photoresist or polyimide. Such use of photoresist or polyimide insulative layers offers distinct advantages over the prior art use of carbon insulative layers. For instance, while carbon is typically applied by vapor deposition techniques, polyimide and photoresist can be applied by spin-on-wafer techniques. Spin-on-wafer techniques enable the polyimide or photoresist to be applied with a relatively planar upper surface. Such planar upper surface can eliminate planarization processes from some applications of the present invention which would otherwise require planarization processes.

Also, spin-on-wafer techniques offer an advantage in that a solvent can be incorporated into a spin-on-wafer applied layer. Such solvent can be vaporized or otherwise removed from the applied layer during vaporization of the applied layer to increase the size or amount of voids formed within the applied layer. The amount of solvent incorporated into a spin-on-wafer applied layer can be controlled by

varying the amount and type of solvent utilized during a spin-on-wafer application of a layer. For instance, a first relatively volatile solvent and a second relatively non-volatile solvent could both be utilized during a spin-on-wafer application. The first solvent would largely evaporate from an applied layer during formation of the layer while the second solvent would substantially remain within the applied layer.

Fig. 9 illustrates a third embodiment of the present invention. In describing the third embodiment, like numerals from the preceding discussion of the second embodiment are utilized, with differences being indicated by the suffix "d" or with different numerals.

Referring to Fig. 9, a wafer fragment 10d comprises a substrate 12d and conductive elements 14d, 16d and 18d overlying substrate 12d. A layer 32d overlies conductive elements 14d, 16d and 18d. Voids 36d are formed between conductive elements 14d, 16d and 18d. Voids 36d can be formed, for example, by methods analogous to those discussed above with reference to Figs. 7 and 8, or by methods utilizing substantially total vaporization of a carbon-comprising material.

Wafer fragment 10d further comprises support members 38 formed between conductive elements 14d and 16d, and between conductive elements 16d and 18d. Support members 38 can advantageously assist in supporting layer 32d over the voids 36d between conductive elements 14d, 16d, and 18d. Support members 38 may comprise either insulative material or conductive material, but preferably do not

comprise a conductive interconnect. Accordingly, support members 38 ar preferably electrically isolated from conductive elements 14d, 16d and 18d, as well as from other conductive structures which may be comprised by an integrated circuit formed on wafer fragment 10d.

Support members 38 can be formed by methods readily apparent to persons of ordinary skill in the art. An example method comprises forming support members 38 between conductive elements 14d, 16d and 18d and subsequently forming a mass, such as mass 30 of Fig. 5 or mass 30c of Fig. 7 between the support members and conductive elements. Layer 32d could be then formed over the mass, over conductive elements 14d, 16d and 18d, and over support members 38. Next, the mass could be either partially or substantially totally vaporized to leave voids, such as voids 36d, between support members 38 and conductive elements 14d, 16d and 18d.

An alternative method of forming support members 38 would comprise forming the support members within an expanse of a mass, such as the mass 30 of Fig. 5, or the mass 30c of Fig.7, by a damascene method.

It is noted that structure 38 may be utilized with either methods of partial vaporization of insulative materials, such as the method described with reference to Figs. 4-6, or with methods of substantially total vaporization of insulative materials, such as the method discussed above with reference to Figs. 7-8.

A fourth embodiment of the present invention is described with reference to Figs. 10-12. In describing the fourth embodiment, like numerals from the preceding discussion of the first embodiment are utilized where appropriate, with differences being indicated with the suffix "e" or with different numerals.

Referring to Fig. 10, a semiconductor wafer fragment 10e is illustrated. Wafer fragment 10e comprises a substrate 12e and conductive elements 14e, 16e, 18e and 40 overlying substrate 12e. A mass 30e is formed over conductive elements 14e, 16e, 18e and 40, as well as between the conductive elements. Mass 30e preferably comprises an insulative material, and can comprise materials such as those discussed above regarding mass 30 (shown in Fig. 4). Mass 30e extends entirely from conductive element 14e to conductive element 16e, entirely from conductive element 16e to conductive element 18e, and entirely from conductive element 18e to conductive element 40.

Referring to Fig. 11, mass 30e is anisotropically etched to remove mass 30e from over conductive elements 14e, 16e, 18e and 40, and to remove mass 30e from between conductive elements 18e and 40. The anisotropic etching forms spacers 42 from mass 30e adjacent conductive element 40 and adjacent conductive elements 14e and 18e.

After the anisotropic, etching mass 30e extends entirely from conductive element 14e to conductive element 16e and entirely from conductive element 16e to conductive element 18e, but no longer extends entirely from conductive element 18e to conductive element 40.

As will b recognized by persons of ordinary skill in the art, methods for anisotropically etching mass 30e will vary depending on the chemical constituency of mass 30e. Such methods will be readily recognized by persons of ordinary skill in the art. An example method for anisotropically mass 30e when mass 30e comprises carbon is a plasma etch utilizing O_2.

A layer 32e is formed over spacers 42, over mass 30e, and over conductive elements 14e, 16e, 18e and 40. Layer 32e preferably comprises a material porous to gas diffusion, such as a silicon dioxide layer having a thickness of about 500 Angstroms or less.

Referring to Fig. 12, mass 30e (shown in Fig. 11) is substantially totally vaporized to form voids 36e. After such substantially total vaporization of mass 30e, spacers 42 comprise an insulative space. Methods for substantially totally vaporizing mass 30e can include methods discussed above with reference to Figs. 8 and 9.

A fifth embodiment of the present invention is described with reference to Fig. 13. In describing the fifth embodiment, like numerals from the preceding discussion of the fourth embodiment are utilized where appropriate, with differences being indicated by the suffix "f" or by different numerals.

Referring to Fig. 13, a wafer fragment 10f is illustrated. Wafer fragment 10f comprises a substrate 12f, and conductive electrical components 14f, 16f, 18f and 40f overlying substrate 12f. An insulative material 32f overlies components 14f, 16f, 18f, 40f, and substrate 12f.

Wafer fragm nt 10f is similar to the wafer fragment 10e of Fig. 12, and may be form d by similar methods. Wafer fragment 10f differs from the wafer fragment 10e of Fig. 12 in that wafer fragment 10f comprises a matrix 34f of partially vaporized material. Matrix 34f can be formed from the mass 30e of Fig. 11 utilizing methods discussed above with reference to Fig. 6. Matrix 34f comprises voids 36f.

Wafer fragment 10f further comprises spacers 42f adjacent conductive elements 14f, 18f and 40f, with spacers 42f comprising matrix 34f and at least one void 36f.

It is noted that in forming the fifth embodiment of Fig. 13, material 32f may be formed either before or after formation of matrix 34f.

A sixth embodiment of the present invention is described with reference to Fig. 14. In describing the sixth embodiment, like numerals from the preceding discussion of the first five embodiments are utilized where appropriate, with differences being indicated by the suffix "g" or by different numerals.

Referring to Fig. 14, a wafer fragment 10g is illustrated. Wafer fragment 10g comprises a substrate 12g and conductive elements 50, 52, 54, 56, 58, 60, 62 and 64. Unlike the first five embodiments, the sixth embodiment of Fig. 14 comprises conductive elements which are vertically displaced from one another, for example, elements 50, 52 and 54, as well as conductive elements which are horizontally displaced from each other, for example, conductive elements 54, 56 and 58. Over

conductive elements 52, 54, 56, 58, 60, 62 and 64 is a gas permeable insulative layer 32g.

Wafer fragment 10g further comprises voids 36g adjacent and between conductive elements 50, 52, 54, 56, 58, 60, 62 and 64. Voids 36g may be formed utilizing the methods discussed above regarding the first five embodiments of the invention. For example, voids 36g may be formed by providing a mass, analogous to mass 30c of Fig. 7, adjacent and between conductive elements 50, 52, 54, 56, 58, 60, 62 and 64, and subsequently substantially totally vaporizing the mass to form voids 36g. Alternatively, voids 36g could be formed within a matrix (not shown) analogous to matrix 34 of Fig. 6 utilizing methods such as those discussed above with reference to Figs. 6 and 13. For instance, a mass analogous to mass 30 of Fig. 5 may be formed adjacent and between conductive elements 50, 52, 54, 56, 58, 60, 62 and 64 and subsequently partially vaporized to form a matrix adjacent and between the conductive elements.

Wafer fragment 10g further comprises support members 70, 72, 74, 76 and 78. Support members 70, 72, 74, 76 and 78 may be formed by methods analogous to the methods discussed above for forming support member 38 with reference to Fig. 9. Support members 70, 72, 74, 76 and 78 preferably comprise sizes and shapes analogous to conductive elements formed at a common elevational level with the support members. Accordingly, support members 70 preferably comprise sizes and shapes analogous to that of conductive element 50; support

members 72 preferably comprise sizes and shapes analogous to that of conductive element 52; support members 74 preferably comprise sizes and shapes analogous to those of conductive elements 54, 56 and 58; support members 76 preferably comprise sizes and shapes similar to that of conductive element 60; and support members 78 preferably comprise sizes and shapes similar to those of conductive elements 62 and 64. Such advantageous similarity of the sizes and shapes of support members with sizes and shapes of conductive elements at similar elevational levels to the support members can advantageously assist in maintaining a substantially planar upper layer 32g.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.